**BHADRAK ENGINEERING SCHOOL & TECHNOLOGY (BEST), ASURALI, BHADRAK**

**COMPUTER SYSTEM ARCHITECTURE (Th- 01)**

**CHAPTER WISE DISTRIBUTION OF PERIODS & MARKS**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Chapter No.** | **Topics** | **Periods as per Syllabus** | **Required period** | **Expected****Marks** |
| 01 | Basic Structure of Computer Hardware | 06 | 07 | 10 |
| 02 | Instruction and Instruction sequencing | 07 | 09 | 15 |
| 03 | Processor System | 10 | 07 | 20 |
| 04 | Memory System | 10 | 11 | 20 |
| 05 | Input-Output System | 10 | 09 | 15 |
| 06 | I/O Interface and Bus Architecture | 10 | 10 | 15 |
| 07 | Parallel Processing | 07 | 07 | 10 |
|  **TOTAL** | **60** | **60** | 105 |

**Sign of Lect. Sign of HOD. Sign of AIC Sign of Vice Principal**

**LESSON PLAN**

|  |  |  |
| --- | --- | --- |
| **Discipline:** **Computer Science Engg.** | **Semester:** Third(3rd ) | **Name of the Faculty:** Er. Jyotsnamayee Jena |
| **Subject:** Computer System Architecture | **No. of days/week class allotted:** Four(4) | **Semester from Date: 0**1.07.24 **to Date:** 08 .11.24**No. of Weeks:** 15 |
| **WEEK** | **CLASS DAY** | **THEORY TOPICS** |
|   1st | 1st | Basic Structure of computer hardware |
| 2nd | Functional Units |
| 3rd | Functional Units Contd. |
| 4th | Computer components |
| 2nd | 1st | Performance measures |
| 2nd | Memory addressing Memory Operations |
| 3rd | **Review Class** |
| 4th | Fundamentals to instructionsOperands Op codes |
| 3rd | 1st | Instruction formats |
| 2nd | Instruction formats contd. |
| 3rd | Instruction formats contd. |
| 4th | **Monthly Test-01** |
|  4th | 1st | Addressing techniques |
| 2nd | Addressing Modes |
| 3rd | Continue… |
| 4th | **Review Class** |
| 5th | 1st | Registers files |
| 2nd | Complete instruction executionFetch |
| 3rd | Decode Execution |
| 4th | Hard wire control  |
| 6th | 1st | Hardwire control contd. |
| 2nd | Micro programmed control |
| 3rd | Micro programmed control contd. |
| 4th | **Monthly Test-02** |
|  7th | 1st | **Review Class** |
| 2nd | Memory characteristics |
| 3rd | Memory – hierarchy |
| 4th | Memory – hierarchy contd. |
| 8th | 1st | Semiconductor RAM organization |
| 2nd | Semiconductor ROM organization |
| 3rd | Interleaved Memory |
| 4th | Cache memory |
| 9th | 1st | Cache memory contd. |
| 2nd | **Monthly Test-03** |
| 3rd | Virtual memory |
| 4th | Virtual memory contd. |
| 10th | 1st | **Review Class** |
| 2nd | Input-Output interface |
| 3rd | Modes of data transfer |
| 4th | Programmed I/O/Transfer |
|  11th | 1st | Interrupt driven i/o |
| 2nd | Interrupt driven i/o contd. |
| 3rd | DMA |
|  4th | **Monthly Test-04** |
| 12th | 1st | DMA contd. |
| 2nd | I/O Processor |
| 3rd | **Review Class** |
| 4th | Bus& system bus |
| 13th | 1st | Types of system Bus – Data bus |
| 2nd | Address bus |
| 3rd | Control Bus |
| 4th | Bus Structure  |
|  14th | 1st | Basic parameter of Bus Design. |
| 2nd | SCSI, USB |
| 3rd | **Review Class** |
| 4th | Parallel Processing |
| 15th | 1st | Linear Pipeline |
| 2nd | Multiprocessor |
| 3rd | Flynn’s Classification |
| 4th | **Review Class** |