**LESSON PLAN**

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| **Discipline:**  Computer Science & Engg. & E&TC Engg | **Semester:**  Third (3rd) | **Name of the Faculty:**  Er Kulamani Jena |
| **Subject:**  Digital Electronics | **No. of days per week class allotted:** Five (5) | **Semester from Date:** 01.07.24 **to Date: 08.** 11.24  **No. of Weeks:** 15 |
| **WEEK** | **CLASS DAY** | **THEORY TOPICS** |
| 1st | 1st | **Introduction** |
| 2nd | Number system: binary, octal, decimal, |
| 3rd | Number system: Hexadecimal, Conversion from one no system to another |
| 4th | Number system: Conversion from one no system to another |
| 5th | Arithmetic operation-Addition, Subtraction, Multiplication, Division. |
| 2nd | 1st | 1’s & 2’s complement of Binary no& subtraction using complement method. |
| 2nd | Digital Code & its application Distinguish between weighted & non-weight Code, |
| 3rd | Binary code,ex-3 code,& gray code |
| 4th | **Logic Gates-** AND, OR, NOT-Symbol, function, expression Truth table & timing diagram |
| 5th | NAND, NOR – Symbol, function, expression Truth table & timing diagram |
| 3rd | 1st | EX-OR & EX-NOR – Symbol, function, expression Truth table & timing diagram |
| 2nd | Universal Gates & its realisation |
| 3rd | Boolean algebra, Boolean expression, DE Morgan’s Theorems |
| 4th | Represent Logic Expression : SOP & POS forms & conversion |
| 5th | **Monthly Test-01** |
| 4th | 1st | Karnaugh’s map (3-4 variable) & minimization of logical expression |
| 2nd | Karnaugh’s map (4 variable) & minimization of logical expression |
| 3rd | Karnaugh’s map (minimization of logical expression, don’t care condition. |
| 4th | **Review** |
| 5th | Half-adders, Full-adder, |
| 5th | 1st | Half subtractor. |
| 2nd | full-Subtractor. |
| 3rd | Serial Binary 4 bit adder |
| 4th | parallel Binary 4 bit adder |
| 5th | Cont. |
| 6th | 1st | Multiplexers (4:1), |
| 2nd | DE multiplexers(1:4) |
| 3rd | Decoder, Encoder |
| 4th | **Monthly test-02** |
| 5th | Digital Comparator(3 bit) |
| 7th | 1st | **Cont.** |
| 2nd | Seven segment decoder |
| 3rd | Cont. |
| 4th | Cont. |
| 5th | **Review class** |
| 8th | 1st | Principles of Flip-Flops operation. Its Types |
| 2nd | S.R. Flip Flop using NAND, Latch un clocked |
| 3rd | S.R. Flip Flop using, NOR Latch un clocked |
| 4th | Cont. |
| 5th | Clocked SR, flip-flop Symbol, logic Circuit |
| 9th | 1st | Clocked, D, T, flip-flop Symbol, logic Circuit |
|  | 2nd | Clocked JK, flip-flop Symbol, logic Circuit |
|  | 3rd | Clocked MS-JK flip-flop Symbol, logic Circuit |
|  | 4th | Clocked logic Circuit |
|  | 5th | **Monthly test-03** |
| 10th | 1st | truth tables, and application |
| 2nd | Concept of Racing and how it can be avoided |
| 3rd | **Review class** |
| 4th | **Shift registers-** SISO, |
| 5th | **Shift registers-** SIPO, PISO |
| 11th | 1st | **Shift registers-** PIPO |
| 2nd | Universal shift register & its application |
| 3rd | Types of Counter & its applications |
| 4th | Binary counter, Asynchronous ripple counters(Up/Down), Decade counter |
| 5th | **Monthly test-04** |
| 12th | 1st | Synchronous counter, Ring Counter |
| 2nd | Concept of memories-RAM, ROM, Static RAM, |
| 3rd | Dynamic RAM, PS RAM |
| 4th | Basic concept of PLD & applications |
| 5th | **Review class** |
| 13th | 1st | Necessity of A/D & D/A Converter |
| 2nd | D/A conversion using Weighted resistor methods |
| 3rd | D/A conversion using R-2R Ladder network |
| 4th | A/D conversion using counter method |
| 5th | A/D conversion using Successive – Approximation method |
| 14th | 1st | **Review class** |
| 2nd | Various logic families & categories according to IC fabrication process |
| 3rd | Characteristics of Digital ICs- propagation Delay, fan-out, fan-in, Power Dissipation, |
| 4th | Noise margin & power supply requirement with reference to logic families |
| 5th | speed with reference to logic families |
| 15th | 1st | Features-Circuit operation & various applications of TTL(NAND) |
| 2nd | CMOS(NAND), CMOS(NOR) |
| 3rd | Review |
| 4th | Previous year question answer discussion |
| 5th | Previous year question answer discussion |